REMARKS

Claims 1-32 remain pending. By this Amendment, claims 1 and 27 are amended to clarify applicants' intention with respect to the claimed subject matter, and to address the Examiner's comments.

The Office Action mailed January 23, 2006 is in substantial part a repeat of the July 27, 2005 Office Action, which was addressed with Applicants' last response filed November 8, 2005. In particular, claims 1-2, 4-10, 14-15, 18 and 20-32 are once again rejected under 35 U.S.C. §102 (e) as being allegedly anticipated by Amparan et al. Claim 19 is rejected under 35 U.S.C. §103 for alleged obviousness over Amparan et al. in view of Das et al. Like the previous Office Action, the current Office Action indicates that claims 3, 11-13 and 16-17 are drawn to allowable subject matter.

The January 23, 2006 Office Action sets forth (at pp. 8-9) new remarks directed to applicants' arguments in support of the claims. It is apparent from those remarks that the Examiner has construed each of independent claims 1 and 27 in a manner contrary to applicants' intention. The amendments to claims 1 and 27 presented herein clarify applicants' intended claim scope and clearly overcome the asserted rejections based upon Amparan et al., as discussed below.

The Remarks appearing at paragraph 22 (pp. 8-9) of the Office Action indicate that the Examiner has interpreted the recited generation of an enhanced set of voltage wireframes to correspond to Amparan et al.'s expansion of trace widths. Applicants have acknowledged that the potential/contour solver approach of Amparan et al. includes an expansion of trace widths within established boundaries. Such a step does not teach or suggest a step or functionality of generating through electronic data processing an enhanced set of voltage wireframes specifying

trace paths which account for stored current requirements of associated components and having no or a reduced quantity of crossover, in the sense that applicants intend. It is intended that the recited enhanced set of voltage wireframes differ from the plurality of initial voltage wireframes in a respect other than trace width, i.e., that the enhanced set of voltage wireframes specify at least one new trace path not included in the plurality of initial voltage wireframes. This is consistent with the separate recitation in each of claims 1 and 27 of a step or functionality of determining a trace width for each segment of the split frame wireframe. In accordance with the claimed inventions of claims 1 and 27 (and the claims depending therefrom), the generation of an enhanced set of voltage wireframes results in the quantity of crossover being reduced or eliminated. This is accomplished by changing the trace paths in some respect, not by increasing a trace width as Amparan et al. do.

As applicants noted in their Remarks submitted with the Amendment filed November 8, 2005, and as described at paragraph 30 of Amparan et al., Amparan et al.'s Fig. 8 grid layout results from application of an auto router. Conventional auto routers, which Amparan et al. apparently employs to arrive at a clean layout in shown in Fig. 8 (lacking crossover), do not take into account current requirements of associated components in routing trace paths. Thus, Amparan et al.'s disclosed process for achieving the layout of Fig. 8 does not teach or suggest the claimed step or functionality of generating an enhanced set of voltage wireframes specifying trace paths which account for stored current requirements of associated components. Amparan et al. teach that the disclosed potential/contour solver approach of Amparan et al.'s first embodiment can be applied to the layout of Fig. 8, to establish boundaries within which trace widths may be expanded. Such trace width expansion is, however, conducted based upon the fixed (clean) layout previously established through use of an autorouter, and does **not** involve

development of any new trace paths (only increasing the width of preexisting trace paths). Thus, Amparan et al. clearly fail to teach or suggest a step or functionality of generating an enhanced set of voltage wireframes as recited, wherein the trace paths specified by the enhanced set of voltage wireframes include at least one new trace path not included in the plurality of initial voltage wireframes.

With Amparan et al.'s approach, the constraints of the voltage potential and gradient threshold set by the user as part of the potential/contour solver approach (Para. [0031]) may not permit a trace width sufficiently large to handle the current requirements for all of the associated components. This is confirmed by para. [0033] of Amparan et al., which describes that "a user may further verify that a trace corresponding to a boundary created using the first method or the second method has a sufficient width and a sufficient resistance to meet design requirements." This comment makes clear that at the time that the layout of Fig. 8 is established, it is unknown whether it will in fact be possible to provide trace widths sufficient to meet the current requirements of the associated components, within the limits established through use of the potential/contour solver approach. In contrast, with the present invention, the need for post-layout verification and correction to ensure that trace widths are adequate to meet current requirements can be avoided, as current requirements are taken into account during the process of creating the enhanced wireframe.

For all of the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. Should the Examiner believe that anything further is desirable in order to place the application in even better form for allowance, he is respectfully urged to telephone applicants' undersigned representative at the below-listed number.

Respectfully submitted,

Christopher L. McKee
Registration No. 32,384

BANNER & WITCOFF, LTD.
1001 G Street, N.W., 11th Floor
Washington, D.C. 20001-4597
(202) 824-3000

Date: 4/14/06

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